SH366307RD/006RDY-BAO00

CONTENTS

1 General Description

SH366307 is a protection IC for lithium-ion/lithium polymer rechargeable batteries, including voltage detection circuits with strict accuracy and delay circuits. It aims for protecting 1-cell lithium-ion/lithium polymer rechargeable battery packs from overcharged, overdischarged, and over-current status.

The SH366307 is a high voltage tolerance CMOS-based protection IC for rechargeable one-cell lithium-ion/ lithium polymer battery,aiming to detect over-charged/over-discharged status of one-cell Li+,along with excessive load current and charge current, protect the battery from the conditions described above. What's more,SH366307 contains short-circuit protector function to prevent excessive short-circuit current.

When the SH366307 detects over-charged voltage or charging over-current, the output of CHG pin switches to "L"(low) level after the internally fixed delay time. When the SH366307 detects over-discharged voltage or discharging over-current, the output of DSG pin switches to "L"(low) level after the internally fixed delay time.

After detecting over-charged voltage, the output of CHG can returns "H"(high) when one of the two following requirements is met:

(1) the cell voltage decreases lower than V_{OVR} (over-charged release voltage);

(2) the cell voltage decreases lower than V_{OV} (over-charged detection voltage),and a discharging current is detected (the load is connected to the circuit).

After detecting over-discharged voltage, the output of DSG pin returns to "H" when one of the two following requirements is met.

(1) The cell voltage increases higher than V_{UVR} (over-discharged release voltage);

(2) the cell voltage gets higher than V_{UV} (over-discharged detection voltage),and a charger is connected.

When the charging over-current is detected,SH366307 will quit the charging over-current status and CHG returns to "H" level if the load circuit is connected.

When the discharging over-current or short-circuit current is detected, SH366307 will quit the discharging over-current or short-circuit status and DSG pin returns to "H" level if the load circuit is removed.

Part.No	V_{OV} **(V)**	V_{OVR} **(V)**	V_{UV} **(V)**	V_{UVR} **(V)**	V_{DOC} **(mV)**	V_{SC} **(mV)**	V_{SC2} **(YES/NO)**	V_{COC} **(mV)**
SH366307RD/006RDY-BAO00	4.600	4.350	2.600	2.900	12.0	30.0	YES	-16.0

续上表:

Part.No	t_{OV} **(s)**	t_{UV} **(ms)**	t_{DOC} **(ms)**	t_{SC} **(μs)**	t_{COC} **(ms)**	0V Battery Charge **(Allowed/ Forbidden)**	Power Down Mode **(YES/NO)**
SH366307RD/006RDY-BAO00	1.0	64	16	280	16	**Forbidden**	**NO**

2 Block Diagram

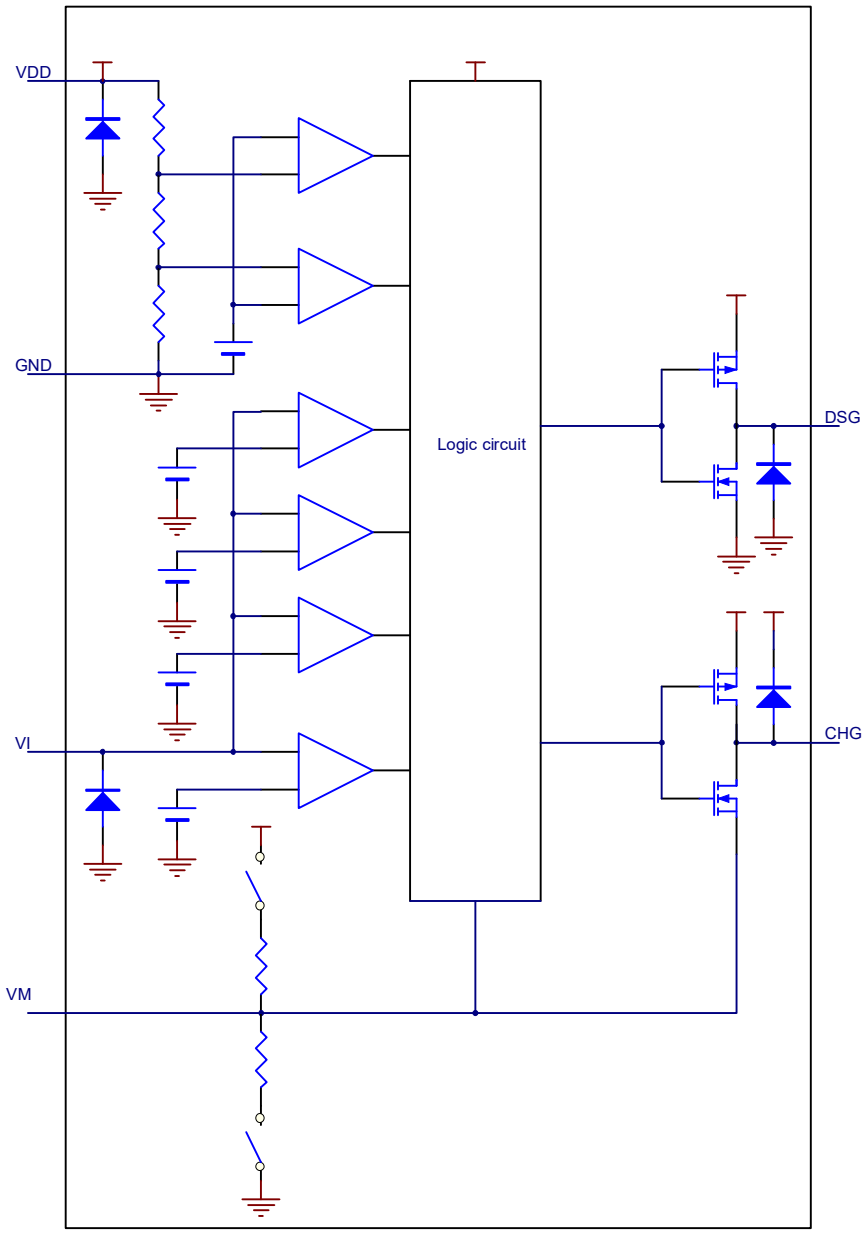


Fig 1. SH366307 Block Diagram

3 Pin Configuration

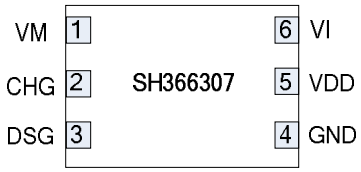


Fig 2. Pin Configuration of SH366307

Table1. SH366307 pin description

Pin NO.	Pin Name	I/O	Function Description
1	VM	I	Load and charger detection pin;
2	CHG	O	Drive pin of charge MOSFET;
3	DSG	O	Drive pin of discharge MOSFET;
4	GND	P	Input pin for negative power supply;
5	VDD	P	Input pin for positive power supply;
6	VI	I	Current detection pin;

Total 6 pins.

4 Absolute maximum ratings

(Ta=25°C,GND=0V)

Item	Pin Name	Absolute Maximum Ratings	Unit
VM pin input voltage	VM	VDD-28 to VDD+0.3	V
CHG pin output voltage	CHG	V_{VM}-0.3 to VDD+0.3	V
DSG pin output voltage	DSG	GND-0.3 to VDD+0.3	V
Input voltage between VDD pin and GND pin	VDD	GND-0.3 to GND+6.0	V
VI pin input voltage	VI	GND-0.3 to VDD+0.3	V
Operation ambient temperature	-	-40 to 85	°C
Storage temperature	-	-55 to 125	°C

Note1: ***If the actual operating parameter exceeds the range of absolute maximum ratings,the components of SH366307 will be permanently damaged. Only when the operating parameters are among the regulated range above, the relevant functions can be guaranteed in normal working status.***

5 Electrical characteristics

5.1 Electrical characteristics(unless otherwise specified, Ta=25°C)

Symbol	Item	Min.	Typ.	Max.	Unit	Testing Circuit
V_{OV}	Overcharge detection voltage	4.580	4.600	4.620	V	A
V_{OVR}	Overcharge release voltage	4.300	4.350	4.400	V	A
t_{OV}	Overcharge detection delay time	0.7	1	1.3	s	B
t_{OVR}	Overcharge release delay time	0.65	1.0	1.5	ms	B
t_{OVHR}	Overcharge hysteresis release delay time	150	250	500	μs	B
V_{UV}	Overdischarge detection voltage	2.550	2.600	2.650	V	A
V_{UVR}	Overdischarge release voltage	2.825	2.900	2.975	V	A
t_{UV}	Overdischarge detection delay time	44.8	64	83.2	ms	B
t_{UVR}	Overdischarge release delay time	0.7	5.0	11.7	ms	B
t_{UVHR}	Overdischarge hysteresis release delay time	0.65	1.0	1.5	ms	B
V_{DOC}	Discharge overcurrent 1 detection voltage	10.5	12.0	13.5	mV	B
t_{DOC}	Discharge overcurrent 1 detection delay time	11.2	16.0	20.8	ms	B
V_{SC}	Short circuit detection voltage	26.0	30.0	34.0	mV	B
t_{SC}	Short circuit detection delay time	196	280	364	μs	B
V_{SC2}	Short circuit 2 detection voltage	VDD-1.4	VDD-0.8	VDD-0.3	V	B
V_{DOCR}	Discharge overcurrent release voltage	0.78*VDD	0.83*VDD	0.86*VDD	V	B
t_{DOCR}	Discharge overcurrent release delay time	0.65	1.0	1.5	ms	B
V_{COC}	Charge overcurrent detection voltage	-17.5	-16.0	-14.5	mV	B
t_{COC}	Charge overcurrent detection delay time	11.2	16	20.8	ms	B
t_{COCR}	Charge overcurrent release delay time	160	250	375	μs	B

Symbol	Item	Min.	Typ.	Max.	Unit	Testing Circuit
V_{CHGH}	CHG output high voltage	VDD-0.15	VDD-0.02	VDD	V	F
V_{DSGH}	DSG output high voltage	VDD-0.15	VDD-0.02	VDD	V	F
V_{LD}	Load detection voltage	0.3	0.35	0.4	V	B
V_{CD1}	Charger detection voltage	GND-0.01	GND	GND+0.01	V	B
V_{0INH}	Minimum battery voltage for charging	0.9	1.5	1.76	V	B
I_{CC}	Current consumption (normal status)	1	2	3	μA	C
I_{UV}	Current consumption in overdischarge status	0.1	0.3	0.5	μA	C
R_{DH}	Internal pull-up resistance of DSG pin	0.5	1.0	1.7	kΩ	D
R_{CH}	Internal pull-up resistance of CHG pin	1.2	2.5	5.0	kΩ	D
R_{DL}	Internal pull-down resistance of DSG pin	2.1	3.1	4.1	kΩ	D
R_{CL}	Internal pull-down resistance of CHG pin	1.6	2.5	4.0	kΩ	D
t_{DH}	The time during the period that the DSG pin rises from GND to VDD-0.5	3	8	15	μs	E
t_{DL}	The time during the period that the DSG pin decreases from VDD-0.5 to GND	10	35	100	μs	E
t_{CH}	The time during the period that the CHG pin rises from the voltage of VM to VDD-0.5	10	25	40	μs	E
t_{CL}	The time during the period that the CHG pin decreases from VDD-0.5 to the voltage of VM	15	47	60	μs	E
R_{VMS}	Internal pull-down resistance of VM pin	7.5	10	15	kΩ	D
R_{VMD}	Internal pull-up resistance of VM pin	0.5	1.25	2.5	MΩ	D

5.2 Electrical characteristics(unless otherwise specified, Ta=-25°C~70°C)

Symbol	Item	Min.	Typ.	Max.	Unit	Testing Circuit
V_{OV}	Overcharge detection voltage	4.575	4.600	4.625	V	A
V_{OVR}	Overcharge release voltage	4.295	4.350	4.405	V	A
t_{OV}	Overcharge detection delay time	0.6	1	1.4	s	B
t_{OVR}	Overcharge release delay time	0.5	1.0	2.0	ms	B
t_{OVHR}	Overcharge hysteresis release delay time	125	250	500	μs	B
V_{UV}	Overdischarge detection voltage	2.545	2.600	2.655	V	A
V_{UVR}	Overdischarge release voltage	2.815	2.900	2.985	V	A
t_{UV}	Overdischarge detection delay time	38.4	64	89.6	ms	B
t_{UVR}	Overdischarge release delay time	0.6	5.0	12.6	ms	B
t_{UVHR}	Overdischarge hysteresis release delay time	0.5	1.0	2.0	ms	B
V_{DOC}	Discharge overcurrent 1 detection voltage	10.0	12.0	14.0	mV	B
t_{DOC}	Discharge overcurrent 1 detection delay time	10.4	16.0	21.6	ms	B
V_{SC}	Short circuit detection voltage	25.5	30.0	34.5	mV	B
t_{SC}	Short circuit detection delay time	168	280	392	μs	B
V_{SC2}	Short circuit 2 detection voltage	VDD-1.4	VDD-0.8	VDD-0.3	V	B
V_{DOCR}	Discharge overcurrent release voltage	0.78*VDD	0.83*VDD	0.86*VDD	V	B
t_{DOCR}	Discharge overcurrent release delay time	0.5	1.0	2.0	ms	B
V_{COC}	Charge overcurrent detection voltage	-18.0	-16.0	-14.0	mV	B
t_{COC}	Charge overcurrent detection delay time	9.6	16	22.4	ms	B
t_{COCR}	Charge overcurrent release delay time	125	250	500	μs	B

Symbol	Item	Min.	Typ.	Max.	Unit	Testing Circuit
V_{CHGH}	CHG output high voltage	VDD-0.15	VDD-0.02	VDD	V	F
V_{DSGH}	DSG output high voltage	VDD-0.15	VDD-0.02	VDD	V	F
V_{LD}	Load detection voltage	0.3	0.35	0.4	V	B
V_{CD1}	Charger detection voltage	GND-0.01	GND	GND+0.01	V	B
V_{0INH}	Minimum battery voltage for charging	0.7	1.5	1.8	V	B
I_{CC}	Current consumption (normal status)	1	2	4	μA	C
I_{UV}	Current consumption in overdischarge status	0.1	0.3	0.8	μA	C
R_{DH}	Internal pull-up resistance of DSG pin	0.5	1.0	1.7	kΩ	D
R_{CH}	Internal pull-up resistance of CHG pin	1.2	2.5	5.0	kΩ	D
R_{DL}	Internal pull-down resistance of DSG pin	2.1	3.1	4.1	kΩ	D
R_{CL}	Internal pull-down resistance of CHG pin	1.6	2.5	4.0	kΩ	D
t_{DH}	The time during the period that the DSG pin rises from GND to VDD-0.5	3	8	15	μs	E
t_{DL}	The time during the period that the DSG pin decreases from VDD-0.5 to GND	10	35	100	μs	E
t_{CH}	The time during the period that the CHG pin rises from the voltage of VM to VDD-0.5	10	25	40	μs	E
t_{CL}	The time during the period that the CHG pin decreases from VDD-0.5 to the voltage of VM	15	47	60	μs	E
R_{VMS}	Internal pull-down resistance of VM pin	7.5	10	15	kΩ	D
R_{VMD}	Internal pull-up resistance of VM pin	0.25	1.25	3.5	MΩ	D

5.3 Electrical characteristics(unless otherwise specified, Ta=-40°C~85°C)

Symbol	Item	Min.	Typ.	Max.	Unit	Testing Circuit
V_{OV}	Overcharge detection voltage	4.565	4.600	4.635	V	A
V_{OVR}	Overcharge release voltage	4.290	4.350	4.410	V	A
t_{OV}	Overcharge detection delay time	0.5	1	1.5	s	B
t_{OVR}	Overcharge release delay time	0.5	1.0	2.0	ms	B
t_{OVHR}	Overcharge hysteresis release delay time	125	250	500	μs	B
V_{UV}	Overdischarge detection voltage	2.540	2.600	2.660	V	A
V_{UVR}	Overdischarge release voltage	2.800	2.900	3.000	V	A
t_{UV}	Overdischarge detection delay time	32	64	96	ms	B
t_{UVR}	Overdischarge release delay time	0.5	5.0	13.5	ms	B
t_{UVHR}	Overdischarge hysteresis release delay time	0.5	1.0	2.0	ms	B
V_{DOC}	Discharge overcurrent 1 detection voltage	10.0	12.0	14.0	mV	B
t_{DOC}	Discharge overcurrent 1 detection delay time	8.0	16.0	24.0	ms	B
V_{SC}	Short circuit detection voltage	25.5	30.0	34.5	mV	B
t_{SC}	Short circuit detection delay time	140	280	420	μs	B
V_{SC2}	Short circuit 2 detection voltage	VDD-1.4	VDD-0.8	VDD-0.3	V	B
V_{DOCR}	Discharge overcurrent release voltage	0.78*VDD	0.83*VDD	0.86*VDD	V	B
t_{DOCR}	Discharge overcurrent release delay time	0.5	1.0	2.0	ms	B
V_{COC}	Charge overcurrent detection voltage	-18.0	-16.0	-14.0	mV	B
t_{COC}	Charge overcurrent detection delay time	8	16	24	ms	B
t_{COCR}	Charge overcurrent release delay time	125	250	500	μs	B

Symbol	Item	Min.	Typ.	Max.	Unit	Testing Circuit
V_{CHGH}	CHG output high voltage	VDD-0.15	VDD-0.02	VDD	V	F
V_{DSGH}	DSG output high voltage	VDD-0.15	VDD-0.02	VDD	V	F
V_{LD}	Load detection voltage	0.3	0.35	0.4	V	B
V_{CD1}	Charger detection voltage	GND-0.01	GND	GND+0.01	V	B
V_{0INH}	Minimum battery voltage for charging	0.7	1.5	1.8	V	B
I_{CC}	Current consumption (normal status)	1	2	4	μA	C
I_{UV}	Current consumption in overdischarge status	0.1	0.3	0.8	μA	C
R_{DH}	Internal pull-up resistance of DSG pin	0.5	1.0	1.7	kΩ	D
R_{CH}	Internal pull-up resistance of CHG pin	1.2	2.5	5.0	kΩ	D
R_{DL}	Internal pull-down resistance of DSG pin	2.1	3.1	4.1	kΩ	D
R_{CL}	Internal pull-down resistance of CHG pin	1.6	2.5	4.0	kΩ	D
t_{DH}	The time during the period that the DSG pin rises from GND to VDD-0.5	3	8	15	μs	E
t_{DL}	The time during the period that the DSG pin decreases from VDD-0.5 to GND	10	35	100	μs	E
t_{CH}	The time during the period that the CHG pin rises from the voltage of VM to VDD-0.5	10	25	40	μs	E
t_{CL}	The time during the period that the CHG pin decreases from VDD-0.5 to the voltage of VM	15	47	60	μs	E
R_{VMS}	Internal pull-down resistance of VM pin	7.5	10	15	kΩ	D
R_{VMD}	Internal pull-up resistance of VM pin	0.25	1.25	3.5	MΩ	D

Note2： ***The current flowing into the chip is negative, such as leak current. The current flowing out of the chip is positive, such as power consumption, pull current.***

Note3： ***Refer to test circuits in chapter 6.***

6 Function Description

6.1 Normal status

When all the following conditions are satisfied, SH366307 is in normal status:

(1). The battery voltage is between V_{UV}(over-discharged detection voltage) and V_{OV}(over-charged detection voltage);

(2). The VI pin voltage of SH366307 is between V_{COC}(charging over-current detection voltage) and V_{DOC} (discharging over-current 1 detection voltage);

(3). CHG pin outputs VDD, DSG pin outputs VDD,charge and discharge MOSFET are both turned on.

6.2 Over-charged status

When all the following conditions are satisfied, SH366307 enters over-charged status and turns off the charge MOSFET:

(1). The battery voltage is higher than V_{OV} (over-charged detection voltage);

(2). The condition of (1) lasts up to t_{OV} (over-charged detection delay time) or longer;

When one of the following conditions is satisfied, the over-charged status is released, and the charge MOSFET is turned on:

(1). The voltage of the VM pin is lower than V_{LD}(without load connection), and the cell voltage is lower than V_{OVR} (over-charged release voltage),lasting up to t_{OVR} (over-charged release delay time) or longer;

(2). The voltage of the VM pin is higher than V_{LD} (with load connection), lasting up to t_{OVHR} (over-charged release hysteresis delay time) or longer, and the cell voltage is lower than V_{OV} (over-charged detection voltage);

Note4： ***When SH366307 is in over-charged status, the discharging over-current detection and short-circuit detection function is disabled.***

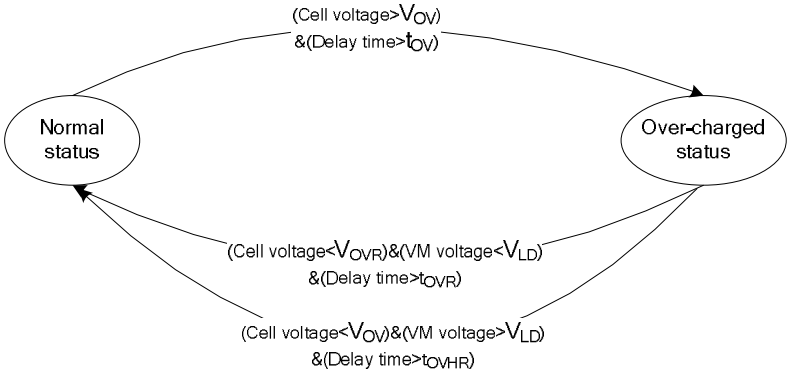


Fig 3. Over-charged Protection

6.3 Over-discharged status

When all the following conditions are satisfied, SH366307 enters over-discharged status and turns off the discharge MOSFET,the internal pull-up resistance is also turned on:

(1). The cell voltage is lower than V_{UV}(over-discharged detection voltage);

(2). The condition (1) lasts up to t_{UV} (over-discharged detection delay time) or longer;

When one of the following conditions is satisfied, the over-discharged status is released, and the discharge MOSFET is turned on:

(1). The voltage of the VM pin is not lower than V_{CD1} (without charger plugged in), and the cell voltage is higher than V_{UVR} ,lasting up to t_{UVR}(delay time of over-discharged release detection);

(2). The voltage of the VM pin is lower than V_{CD1} (with charger plugged in),lasting up to tUVHR (delay time of over-discharged release hysteresis) or longer, and the cell voltage is higher than VUV(over-discharged detection voltage);

Note5： ***When cell voltage is lower than V_{UV}, the charging overcurrent detection function is disabled.***

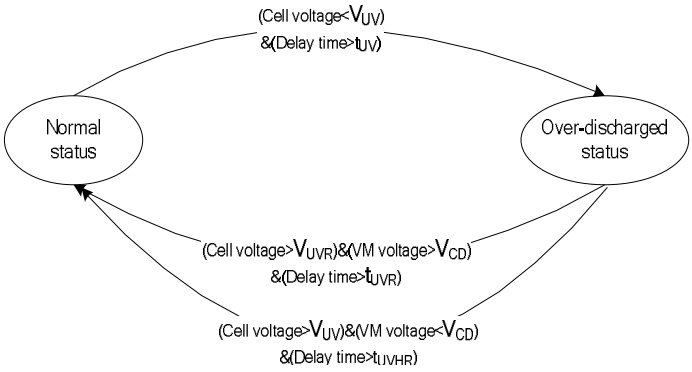


Fig 4. Overdischarge Protection

6.4 Power Down status

The Power Down Mode is disabled in this code(SH366307-BAO00).

6.5 Discharging over-current status

SH366307 has three levels for discharging over-current protection, V_{DOC} (discharging over-current 1 detection voltage) is lower than V_{SC}(short-circuit detection voltage), t_{DOC} (delay time of discharging over-current detection 1) is larger than t_{SC} (short-circuit detection delay time).

When all the following conditions are satisfied, SH366307 enters discharging over-current status and turns off the discharge MOSFET:

(1). The VI pin voltage of SH366307 is higher than V_{DOC}/V_{SC};

(2). The condition of (1) lasts up to t_{DOC}/t_{SC} or longer;

When all the following conditions are satisfied, the discharging over-current status is released:

(1). Load is disconnected or charger is connected(the VM voltage is lower than V_{DOCR});

(2). The condition of (1) lasts up to the t_{DOCR} (delay time of discharging over-current release)or longer.

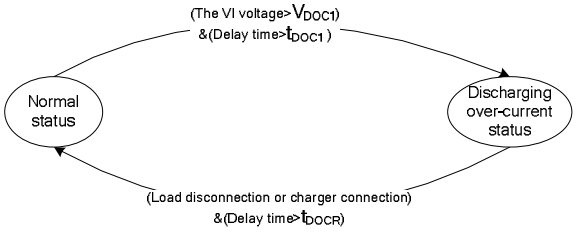


Fig 5. Discharging over-current 1 Protection

Note6： ***When SH366307 is in discharging over-current status, SH366307 will turn on the internal pull-down resistance and pull VM pin down to GND,in order to judge whether the outside load is removed.***

6.6 Discharging short-circuit 2 status

SH366307 contains discharging short-circuit 2 protection,when both of the following conditions are satisfied,system enters

discharging short-circuit 2 status and turns off the discharge MOSFET:

(1). The VM pin voltage is higher than V_{SC2}(discharging short-circuit 2 detection voltage);

(2). The condition (1) lasts up to t_{SC};

When all the following conditions are satisfied, the discharging short-circuit 2 status is released:

(1). The load is disconnected or the charger is connected(the voltage of VM pin is lower than V_{DOCR});

(2). The condition (1) lasts up to t_{DOCR};

6.7 Charging over-current status

SH366307 contains charging over-current protection function, when all the following conditions are satisfied, system enters charging over-current status and turns off the charge MOSFET:

(1). The VI pin voltage of SH366307 is lower than V_{COC}(charging over-current detection voltage);

(2). The condition of (1) lasts longer than t_{COC}(delay time of charging over-current detection);

When all the following conditions are satisfied, the charging over-current status is released:

(1). The load is connected (the voltage of the VM pin is higher than V_{LD});

(2). The condition of (1) lasts longer than t_{COCR}(delay time of charging over-current release);

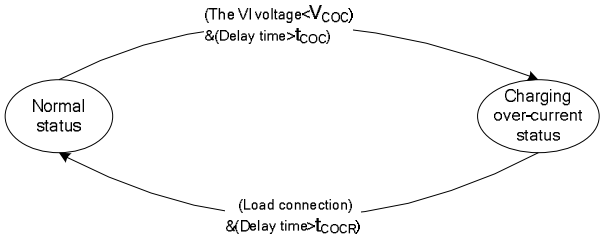


Fig 6. Charging over-current Protection

6.8 Function for 0V battery charging

When the battery voltage decreases lower than V_{0INH}, the charge MOSFET will be turned off to inhibit charging.

7 Test Circuits

7-1 Overcharge detection voltage (V_{OV}) & Overcharge release voltage(V_{OVR})

【Test Circuit】: A

【Description】: Set V1=3.4V, V2=0V,connect VI pin to GND. Increase V1 until the voltage of CHG pin drop to low,the present V1 is V_{OV}.Then decrease V1 from present voltage,until the voltage of CHG pin returns to normal,similarly,is V_{OVR} .

7-2 Overdischarge detection voltage (V_{UV}) & Overdischarge release voltage (V_{UVR})

【Test Circuit】: A

【Description】: Set V1=3.4V, V2=0.1V,connect VI pin to GND.Decrease V1 until the voltage of DSG pin drop to low, the present V1 is V_{UV} .Then Increase V1 from present voltage,until DSG pin returns to normal,similarly,is V_{UVR} .

7-3 Discharge overcurrent 1 detection voltage (V_{DOC})

【Test Circuit】: B

【Description】: Set V1=3.4V,V5=0V,disconnect VM from V2,connect switch1.Increase V5 until the following two requirements are satisfied.Then,the present V5 is V_{DOC}.

(1)The DSG pin shuts down;

(2)The delay time between the rise of V5 and shutting down of DSG is aroud 16ms.

7-4 Short circuit detection voltage(V_{SC})

【Test Circuit】: B

【Description】: Set V1=3.4V,V5=0V,disconnect VM from V2,connect switch1.Increase V5 until the following two requirements are satisfied.Then,the present V5 is V_{SC}.

(1)The DSG pin shuts down;

(2)The delay time between the rise of V5 and shutting down of DSG is aroud 280μs.

7-5 Short circuit detection voltage(V_{SC2})/ Discharge overcurrent release voltage (V_{DOCR})

【Test Circuit】: C

【Description】: Set V1= VDD-1=3.4V,V2=V5=0V.Increase V2 until DSG pin shuts down,the present V2 is V_{SC2}.Then decrease V2 to 0V,decrease VDD-1 of the extra test circuit until DSG pin returns high,similarly,is $V_{DOCR.}$

7-6 Charge overcurrent detection voltage (V_{COC})

【Test Circuit】: B

【Description】: Set V1=3.4V,V2=V5=0V,disconnect switch1.Decrease V5 until CHG pin shuts down.Then,the present V5 is V_{COC}.

7-7 Load detection voltage (V_{LD})

【Test Circuit】: B

【Description】: Set V1=4.7V,V2=V5=0V,disconnect switch1,the CHG pin turns low,then decrease V1 to 4.31V .Increase V2 till the point where CHG returns high.The present V2 is V_{LD}.

7-8 Charger detection voltage (V_{CD1})

【Test Circuit】: B

【Description】: Set V1=2.0V,V5=0V,V2=0.1V,disconnect switch1,the DSG pin turns low.Then increase V1=2.75V.Decrease V2 gradually,if V2 is decreased to 0V while DSG still keeps low,then continue decrease V2 to negative(adjustment step is 1mV),till the DSG returns high.The present V2 is the V_{CD1}.

7-9 Operating current in normal mode(I_{CC})
【Test Circuit】: C
【Description】: Set V1=3.4V,V5=V2=0V, remove the extra test circuit of DSG.Record the current at IC's VDD pin.

7-10 Current consumption of over-discharged status (I_{UV})
【Test Circuit】: C
【Description】: Set V1 =1.8V, V5=0V, disconnect V2, remove the extra test circuit of DSG.DSG pin turns down.Record the current at IC's VDD pin,which is $I_{uv.}$

7-11 Internal pull-down resistance of VM pin (R_{VMS})
【Test Circuit】: D
【Description】: Set V1=V2=3.4V,V5=0V,remove V3 and V4.DSG pin turns low.Record the current at IC's VM pin I_{VM},then calculate the result: R_{VMS}=V2/ I_{VM}.

7-12 Internal pull-up resistance of VM pin (R_{VMD})
【Test Circuit】: D
【Description】: Set V1=2.0V,V2=V5=0V,remove V3 and V4.Record the current at IC's VM pin I_{VM},and calculate the R_{VMD}=V1/I_{VM}.

7-13 Internal pull-up resistance of DSG pin (R_{DH})
【Test Circuit】: D
【Description】: Set V1=4.0V,V2=V5=0V,V3=V4=3.5V, obtain the current flowing out the DSG pin I_{DO}.R_{DH}=0.5V/ $I_{DO.}$

7-14 Internal pull-up resistance of CHG pin (R_{CH})
【Test Circuit】: D
【Description】: Set V1=4.0V,V2=V5=0V,V3=V4=3.5V, obtain the current flowing out the CHG pin I_{CO}. R_{CH}=0.5V/ $I_{CO.}$

7-15 Internal pull-down resistance of DSG pin (R_{DL})
【Test Circuit】: D
【Description】: Set VDD=2.2V,V2=V5=0V,V4=0.1V, system enters over-discharge protection system and DSG pin turns down.Obtain the current sinking into the DSG pin I_{CO}.R_{DL}=0.1V/ $I_{CO.}$

7-16 Internal pull-down resistance of CHG pin (R_{CL})
【Test Circuit】: D
【Description】: Set VDD=4.7V,V2=V5=0V,V3=0.1V, system enters over-charge protection system and CHG pin turns down.Obtain the current sinking into the CHG pin I_{CO}.R_{DL}=0.1V/ $I_{CO.}$

7-17 Overcharge detection delay time (t_{OV})
【Test Circuit】: B
【Description】: Set V1=3.4V, V2=V5=0V,system operates in normal status.Then change V1 swiftly to 4.7V,the delay time between the point where V1 is higher than the actual V_{OV} and shutting down of CHG is exactly the t_{OV}.

7-18 Overdischarge detection delay time (t_{UV})
【Test Circuit】: B
【Description】: Set V1=3.4V, V2=V5=0V,disconnect switch1,system operates in normal status.Then change V1 swiftly to 2.0V,the delay time between the point where V1 is lower than the actual V_{UV} and shutting down of DSG is exactly the t_{UV}.

7-19 Discharge overcurrent 1 detection delay time (t_{DOC})
【Test Circuit】: B
【Description】: Set V1=3.4V, disconnect VM from V2,connect switch1.Set V5=15.0mV,connect VI to V5 swiftly,the delay

time between the rise of VI and shutting down of DSG is exactly the $t_{DOC.}$

7-20 Short circuit detection voltage (t_{SC})

【Test Circuit】: B

【Description】: Set V1=3.4V, disconnect VM from V2,connect switch1.Set V5=35mV,connect VI to V5 swiftly,the delay time between the rise of VI and shutting down of DSG is exactly the $t_{SC.}$

7-21 Charge overcurrent detection delay time (t_{COC})

【Test Circuit】: B

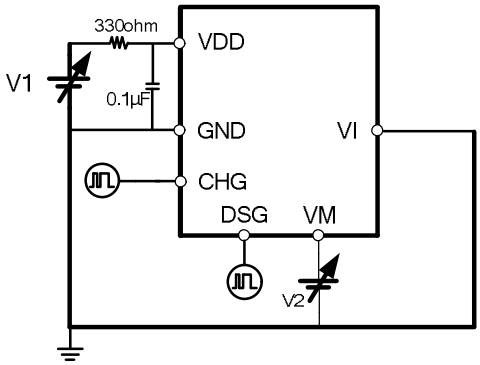
【Description】: Set V1=3.4V,V2=0V,disconnect switch1.Set V5=-18mV,connect VI to V5 swiftly,the delay time between the drop of VI and shutting down of CHG is exactly the $t_{COC.}$

7-22 Minimum battery voltage for charging (V_{0INH})

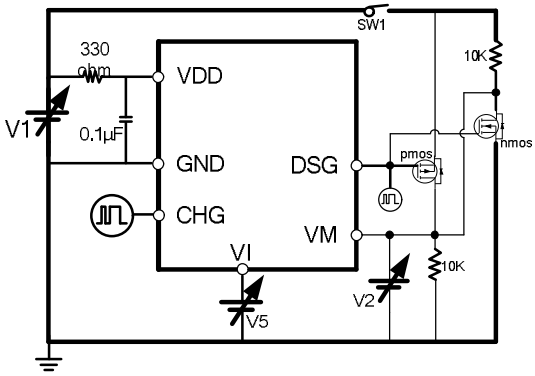
【Test Circuit】: B

【Description】: Set V1=1.8V,V2=0V,V5=0V,disconnect switch1.Decrease V1 till the point where CHG turns down.The present V1 is V_{0INH}.

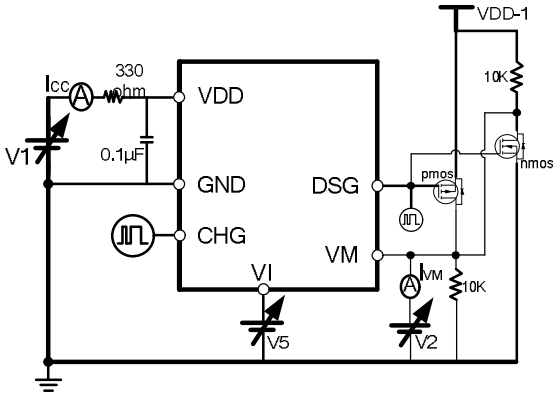
Note7: ***When testing 7-3(V_{DOC}),7-4(V_{SC}),7-6(V_{SC2}&V_{DOCR}),7-19(t_{DOC}), 7-20(t_{SC}),the VDD-1 will be adjusted only in 7-6,so we should add another 3.4V to VDD-1,in the other items,the VDD-1 can be connected to V1 directly for convenience.***



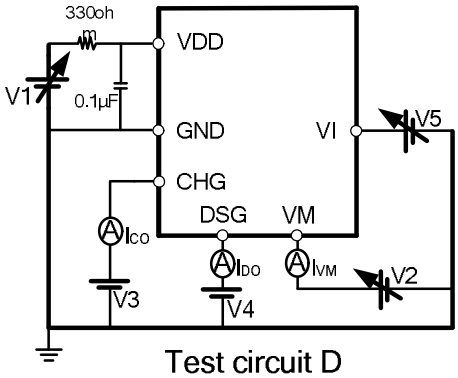
Test circuit A



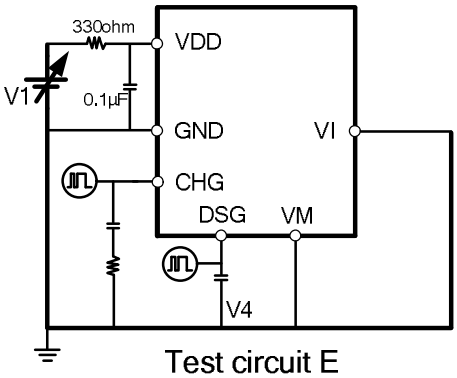
Test circuit B



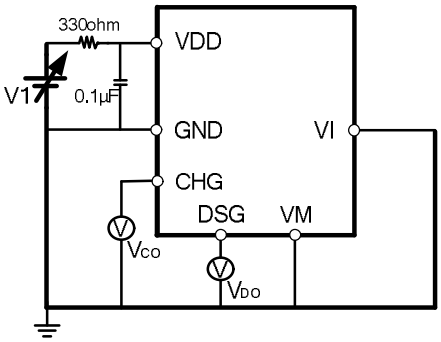
Test circuit C



Test circuit D



Test circuit E



Test circuit F

8 Typical application schematic

8.1 Application schematic of SH366307

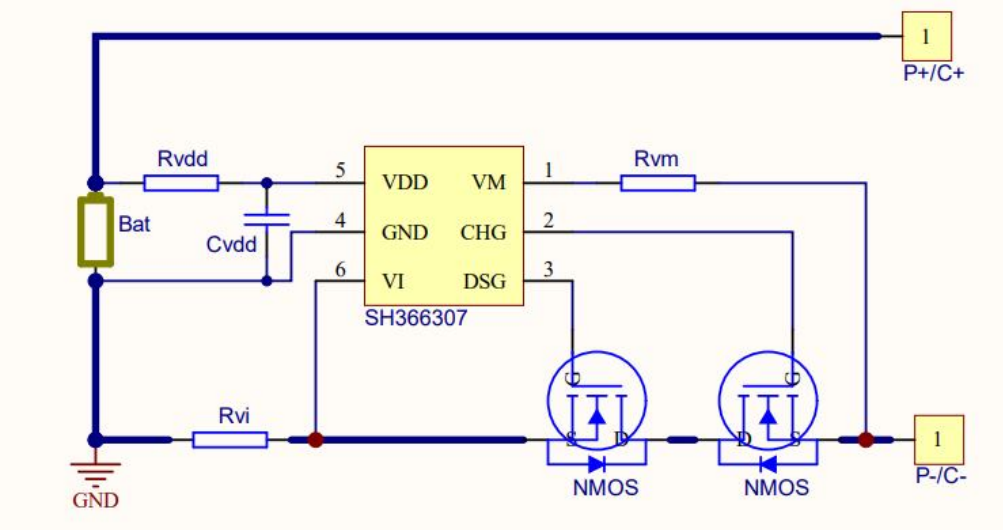


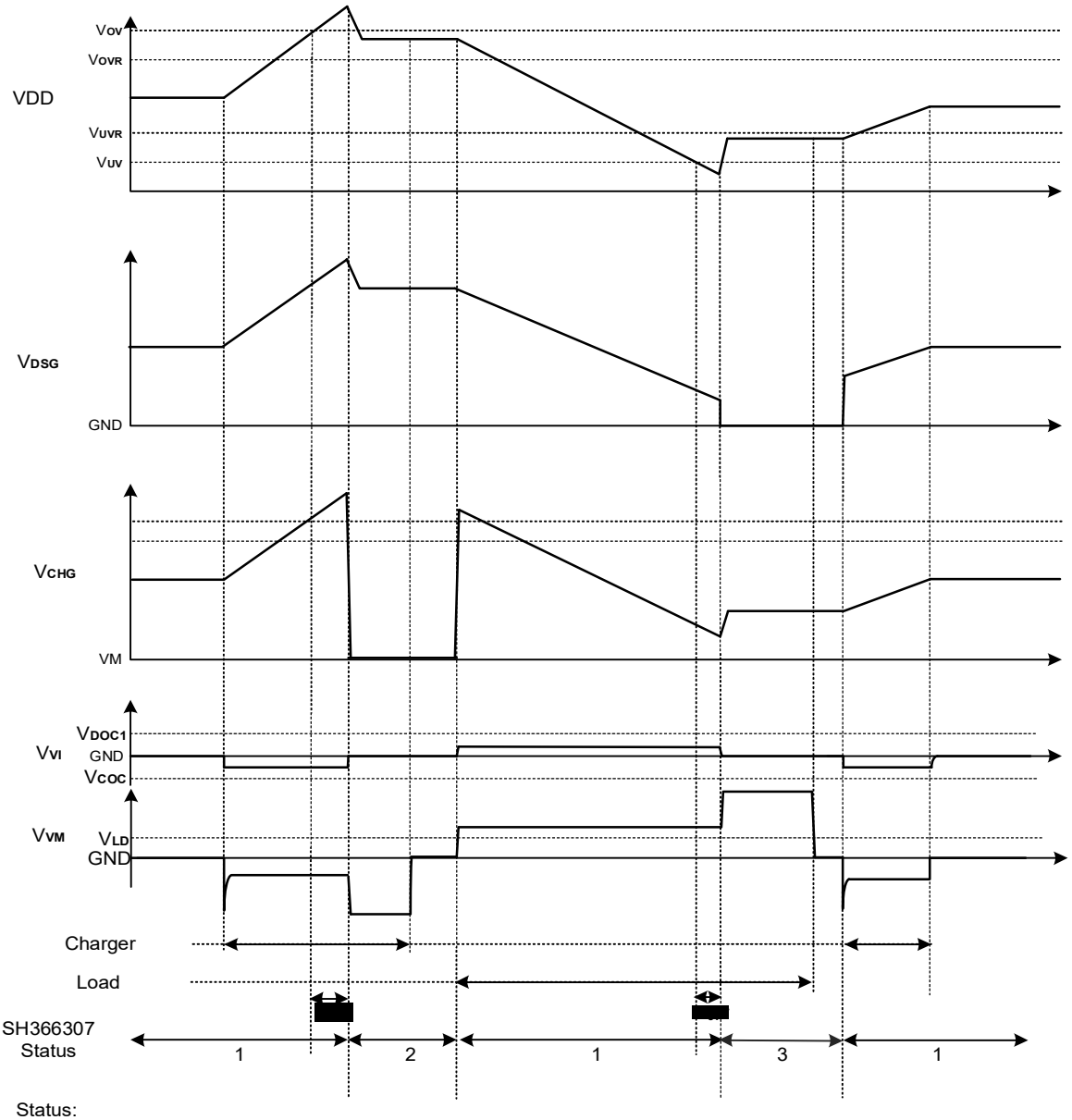
Fig 8. Application schematic of SH366307

8.2 External Components

	Symbol	Min.	Typ.	Max.	Unit
1	R_{vdd}	100	330	1000	Ω
2	C_{vdd}	0.068	0.1	1	μF
3	R_{vm}	100	470	1000	Ω
4	R_{Vi}	1	3	20	mΩ

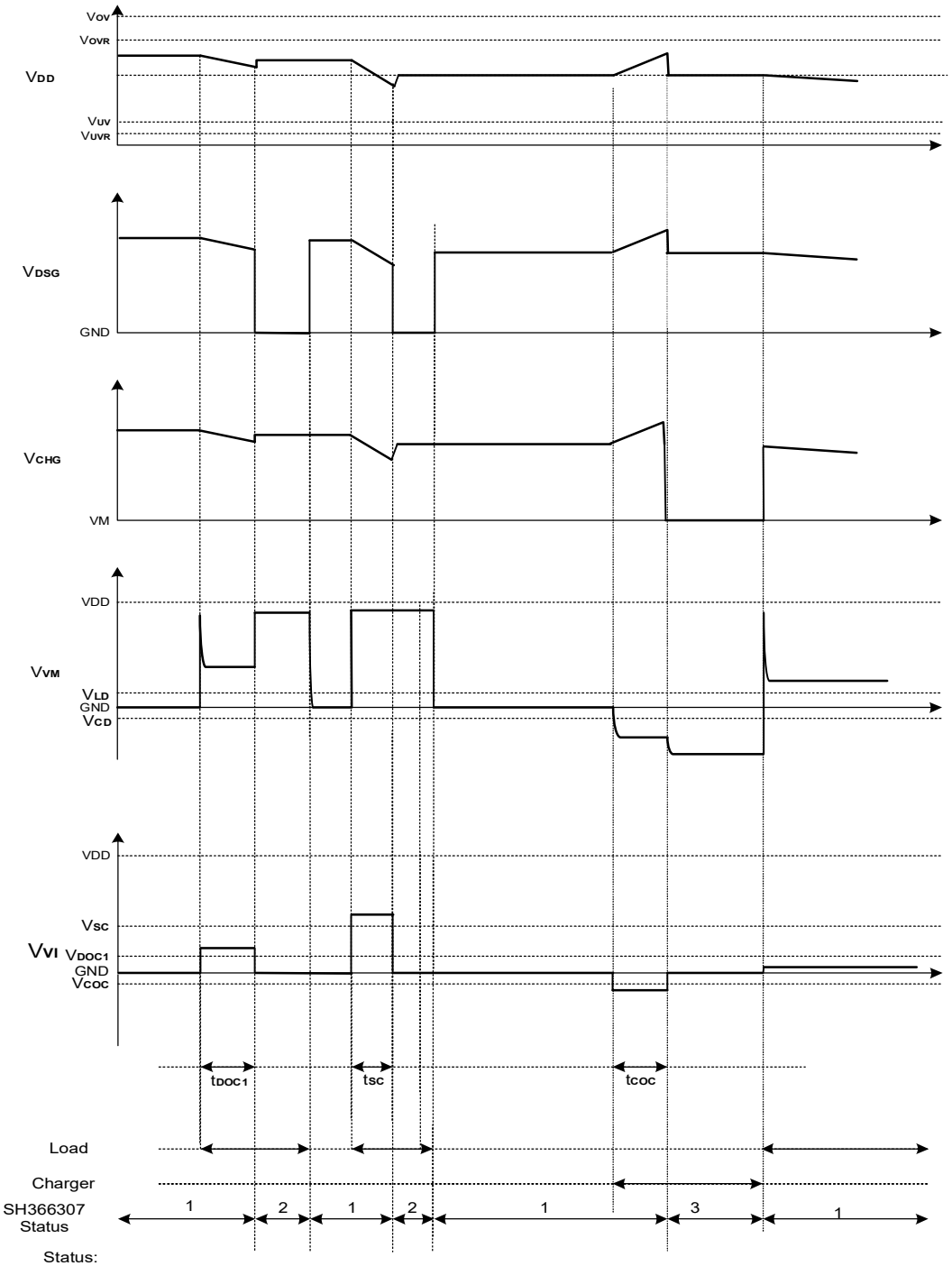
9 Timing Chart

9.1 Over-voltage and Under-voltage Operation



Status:
1.Normal status;
2.Over-charged status;
3.Over-discharged status;
tov:Delay time of over-charged detection;
tuv:Delay time of over-discharged detection;

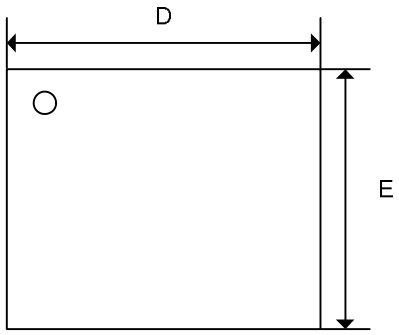
9.2 Over-current Operation



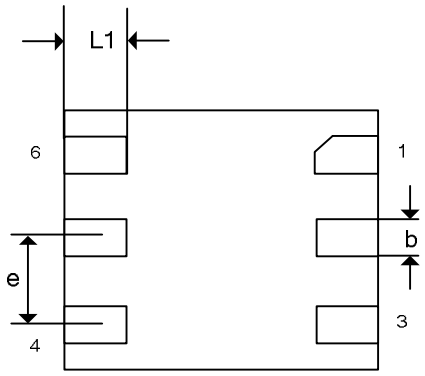
Status:
1.Normal status;
2.Discharging over-current status;
3.Charging over-current status;
t_{DOC1}/t_{COC}:Delay time of Discharging/Charging over-current;
t_{SC}:Delay time of short-circuit;

10 Package dimensions

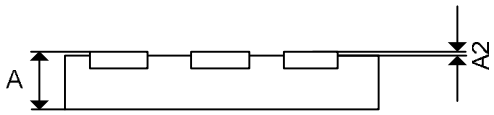
DFN 6L (1.57 X 1.9) (P0.50 T 0.37) Outline Dimensions **unit: mm**



Top View



Bottom View



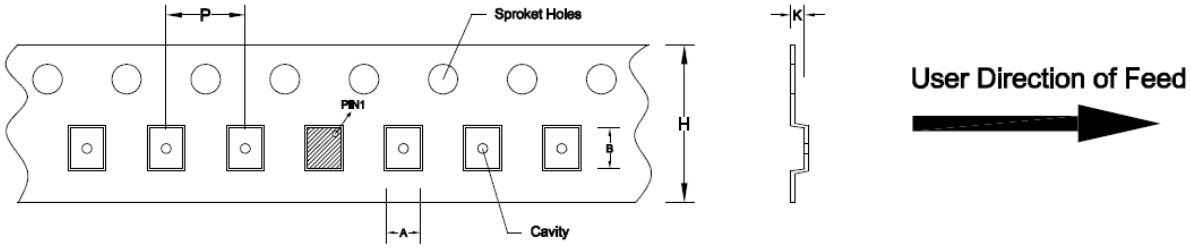
Side View

Symbol	Dimensions in mm		
	MIN	NOR	MAX
A	0.34	0.37	0.40
A2	0	0.025	0.05
D	1.8	1.9	2.0
E	1.47	1.57	1.67
b	0.17	0.22	0.27
e	0.5TYP		
L1	0.25	0.30	0.35

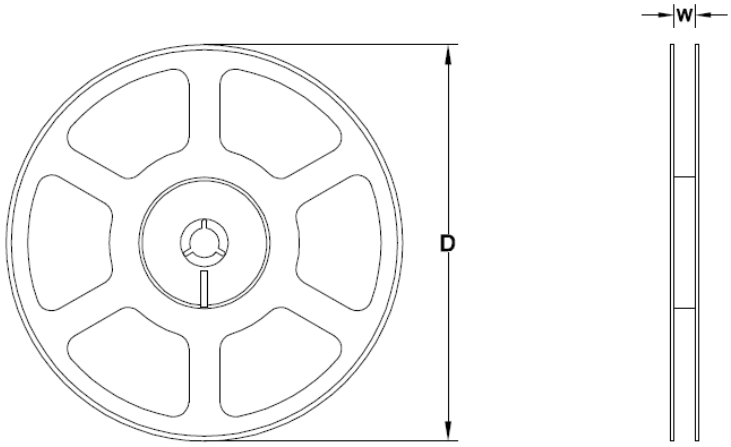
11 Carrier Tape and Reel Information

DFN6L（1.57*1.9） **unit：mm**

Carrier Tape Dimensions



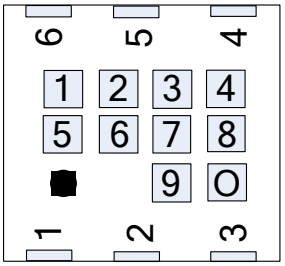
Reel Dimensions



*All dimensions are **nominal**

A	1.71	Dimension designed to accommodate the component width
B	2.08	Dimension designed to accommodate the component length
K	0.71	Dimension designed to accommodate the component thickness
H	8	Overall width of the carrier tape
P	4	Pitch between successive cavity centers
W	8.4	Reel width
D	178	Reel diameter

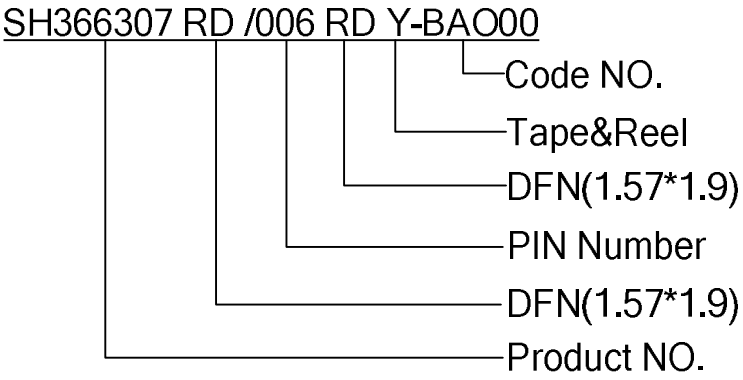
12 Mark Specification



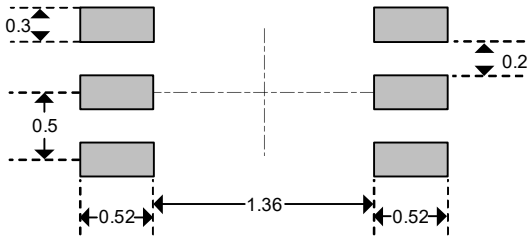
Top view

①~④：Product abbreviations（6BAO）;
⑤~⑧：Lot Number;
Last row: Year & month

13 Product Name Structure



14 Pad size



Unit：mm

15 Modification record

Modification record of SH366307（BAO）		
Detailed description	**Located pages**	**Date**
Original version V0.0	-	2022/4/02
Modify the test method of 7-1、7-2、7-9and 7-10	P14、P15	2022/06/08
Revise the package dimensions	P22	2022/10/12
Change the max value of V0INH in the sheet	P6/8/10	2022/10/18
Add Pad size	P23	2023/3/9

IMPORTANT NOTICE

This manual is the property of Sino Wealth Electronic Ltd. and its affiliates ("Company"). This manual, including all of the Company's products ("Products") described herein, is owned by the Company according to relevant laws or treaties. The Company reserves all rights under such laws and treaties, and does not grant you any license to use its patents, copyrights, trademarks and other intellectual property rights.

Any technical information in this manual, including functional descriptions and schematic diagrams, shall not be construed as a license to use or exercise any intellectual property rights. The names and brands (if any) of the relevant third parties are quoted in this manual are the property of their respective owners, for identification purposes only.

The Company does not make any warranty, expressed or implied, about this manual or any Product, including, but not limited to, implied warranties of merchantability and fitness for a particular purpose. The Company shall not be liable for any use of any of Product described in this manual out of its specifications or the Company's standard. Except for the special Products specified in the applicable agreement, the Products are designed, developed and manufactured for general commercial, industrial, personal and/or domestic applications only. In particular, the Products are prohibited to be used in following fields, such as military, national defense, nuclear energy, medical treatment and others that may cause personal injury, death or environmental damage. Users shall take all actions to ensure that the Products are used and sold in accordance with applicable laws and regulations.

The failure or malfunction of semiconductor products may occur. Users of the Products should therefore give thorough consideration to safety design, including redundancy, fire-prevention measures and etc., to prevent any accidents, fire or community damage that may ensue. Especially, the reference application circuit is not guaranteed to be suitable for the specific application of mass production.

In the event that users breach the above statement, the Company shall not be liable in whole or in part, and users shall hereby release the Company and its -agents and/or distributors from any claim, damage or other liability; At the same time, users shall indemnify the Company and its agents and/or distributors against all claims, costs, damages and other liabilities, including claims for personal injury or death, arising out of any unintended use of the Product.

The information in this manual is related to the Product only. The Company reserves the right to make changes, modifications or improvements to this manual, the Products and services described herein at any time without prior notice. Users are advised to contact our sales department before purchase.

The Company has the final right to interpret this manual.